

DEFENCE AND SPACE
Space Products

NEMO-2 2041

High-End Non-Volatile
Mass Memory



P a y l o a d

D a t a H a n d l i n g



The NEMO-2 2041 is a compact solid-state recorder that provides high-end mass memory storage and performance to Earth observation missions. This product is the result of over 30 years, where Airbus Defence and Space has gained a strong flight heritage on solid-state technologies.

First model of NEMO-2's modular and scalable architecture, it is based on qualified building blocks packaged in a slice form factor.

This mass memory provides straightforward and simultaneous record and replay capability using Flash technology.

NEMO-2 2041 is a redundant unit, made of two identical MEMORY slices with their dedicated DC/DC converters.

The NEMO's 2041 configuration has a user capacity of 4Tbits.

First Flight Models by End 2023.

Architecture and key features

- The unit is composed of an assembly of 2 identical cold-redundant slices
- Each slice is self-contained and with its own external interfaces for inputs, outputs, power and control
- Each slice embeds a memory bank of 4Tbits and state-of-the-art processing capabilities built on a rad-tolerant FPGA coupled with a rad-hard processor

INTERFACES	
FROM/TO SATELLITE MANAGEMENT UNIT	Primary power input, unregulated redundant power bus 22-38V Redundant MIL-STD-1553B for TM/TC command and telemetry purpose Power on/off status, secondary voltage telemetry and thermistor telemetry interface
RECORD INTERFACES	2x Nominal + 2x Redundant High Speed WizardLink Instrument Record Interfaces, data rate up to 2Gbps on each link 2x Nominal + 2x Redundant SpW Instrument Record Interfaces, data rate up to 200Mbps on each link 1x Nominal + 1x Redundant SpW links for housekeeping, data rate up to 100kbps
REPLAY INTERFACES	3x High Speed Wizardlink Replay interfaces with flow control, 2 active at a time, data rate up to 2Gbps on each link

MAIN FUNCTION	KEY FEATURES														
<ul style="list-style-type: none"> √ Non volatile Payload and Platform Data Storage (spacecraft housekeeping/ancillary,...) √ Simultaneous record & replay are possible at highest data rates √ Provision of discrete telemetries (power status, internal temperatures & secondary operating voltages) 	<table border="1"> <tbody> <tr> <td>GENERIC SERVICES</td> <td>PUS-C services</td> </tr> <tr> <td>MEMORY</td> <td>Large capacity non-Volatile Flash Memory Array composed of the second generation of Airbus qualified flash components CCSDS files based operations (FBO)</td> </tr> <tr> <td>PROCESSING</td> <td>High performance FPGA SCOC3 System-On-Chip based on the LEON3 sparc v8 core</td> </tr> <tr> <td>CHANNEL CODING</td> <td>CCSDS Packet Telemetry Standard Transmission over Virtual Channels CADU generator for Formatting of playback TM files CFDP (CCSDS File Delivery Protocol) Class 1 & 2 for downlink</td> </tr> <tr> <td>ARCHITECTURE LEVEL</td> <td>Unit free of single point failure 2x cold-redundant identical slices Record and replay interfaces externally cross-strapped</td> </tr> <tr> <td>DESIGN LEVEL</td> <td>Flash wear levelling & bad blocks management The memory array is designed to allow the loss of up to two memory components Protected from data errors induced by SEU/MEU by symbol error correction</td> </tr> <tr> <td>PART LEVEL</td> <td>Radiation hardened Processor Radiation tolerant FPGA Usage of latch up free parts High efficiency internal DC/DC converter with protected features</td> </tr> </tbody> </table>	GENERIC SERVICES	PUS-C services	MEMORY	Large capacity non-Volatile Flash Memory Array composed of the second generation of Airbus qualified flash components CCSDS files based operations (FBO)	PROCESSING	High performance FPGA SCOC3 System-On-Chip based on the LEON3 sparc v8 core	CHANNEL CODING	CCSDS Packet Telemetry Standard Transmission over Virtual Channels CADU generator for Formatting of playback TM files CFDP (CCSDS File Delivery Protocol) Class 1 & 2 for downlink	ARCHITECTURE LEVEL	Unit free of single point failure 2x cold-redundant identical slices Record and replay interfaces externally cross-strapped	DESIGN LEVEL	Flash wear levelling & bad blocks management The memory array is designed to allow the loss of up to two memory components Protected from data errors induced by SEU/MEU by symbol error correction	PART LEVEL	Radiation hardened Processor Radiation tolerant FPGA Usage of latch up free parts High efficiency internal DC/DC converter with protected features
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PERFORMANCE PARAMETERS															
User memory capacity: 4Tbits EOL Aggregated record + replay data rate: up to 8Gbits/s															
RELIABILITY & PERFORMANCE VS ENVIRONMENT															
Life time: 7.5 years in LEO orbit EEE Quality: Class 1 or Class 2 Operating range: -30°C to +60°C NAND flash endurance: Minimum 60K Program/ Erase cycles Residual Bit error rate: $<5.3 \times 10^{-17}$ error/bit/day for mission Vibration: 24g sine; 15g rms random out of plane Shock: 1000g at 1600Hz Reliability: 0.997 covering 7.5 years in-orbit at 35°C	<table border="1"> <thead> <tr> <th>BUDGETS</th> </tr> </thead> <tbody> <tr> <td>Mass: 9kg Size L x H x W (mm): 365 x 225 x 176 Power dissipation: <30W peak (with simultaneous Record & Replay at maximum data rate)</td> </tr> </tbody> </table>	BUDGETS	Mass: 9kg Size L x H x W (mm): 365 x 225 x 176 Power dissipation: <30W peak (with simultaneous Record & Replay at maximum data rate)												
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